

Applicants: Anatoliy V. Tsyrganovich  
Serial No.: 10/690,874  
Filing Date: October 21, 2003  
Docket No.: ZIL-521-1P

**Amendments to the Specification:**

Please replace paragraph [0001] with the following replacement paragraph.

[0001] The present application is a continuation-in-part of and claims the benefit under 35 U.S.C. §120 from U.S. patent application serial number 09/973,979, now U.S. Patent No. 6,636,122 B2, filed October 9, 2001. The entire subject matter of U.S. patent application serial number 09/973,979 is incorporated herein by this reference.

Please replace paragraph [0027] with the following replacement paragraph.

[0027] FIG. 1 shows an embodiment of a frequency locked loop 160. The frequency locked loop as shown comprises two sections: a voltage-controlled oscillator 162 for generating an output clock signal 166, and a feedback circuit 164 for providing a correction signal 168 to control the frequency of the output clock signal 166 generated by the voltage-controlled oscillator 162. The frequency locked loop 160 is provided with a system clock signal 170 running at exactly ~~at~~ a required frequency by a system clock generator or MRO (master reference oscillator) 172. The system clock is sometimes termed a reference clock, and some systems may have more than one system clock and/or reference clock. It should be noted that the system clock signal 170 is not synchronized with the synchronizing signal 174. The system clock signal 170 is, however, running at exactly the required output clock frequency.

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Thus, this frequency locked loop 160 is designed to generate the synchronized output clock signal 166 running at the same frequency as that of the system clock signal 170 while also having an edge synchronized with the synchronizing signal 174. Synchronizing signal 174 is provided by external SYNC signal source 173 which need not be coherent.

Please replace paragraph [0039] with the following replacement paragraph.

[0039] FIG. 4 shows a block diagram of a digital conversion circuit used to generate feedback signal 168 according to an aspect of the invention. Digital conversion circuit 340 has two pulsed inputs, gauge signal G1 196, and gauge signal G2 198. Digital conversion circuit 340 also receives system clock signal 170. Digital conversion circuit 340 has one output, analog feedback correction signal 168. Each of the pulses carried by gauge signals G1 196 and G2 198 has a rising edge and a falling edge. Because gauge signal G2 198 is locked to the external synchronization signal 174 (FIG. 2), it will have a rising edge that occurs prior to or simultaneously with the rising edge of the corresponding pulse carried by gauge signal G1 196.

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Please replace paragraph [0070] with the following replacement paragraph.

[0070] The difference between the two digital values stored in registers 631 and 632 is indicative of the magnitude of the difference in frequency between the FEEDBACK CLOCK and the REF CLOCK. More particularly, it is indicative of the time difference between the period of time 644 that the feedback clock signal is high and the period of time 645 that the reference clock is low. Accordingly, the value in register 631 is converted into a base two number by block 633 and the result is supplied to subtractor 635. The value in register 632 is converted into a base two number by block 634 and the result is supplied to subtractor 635. Subtractor 635 outputs the difference between the two values and supplies this difference to digital filter 636. By subtracting the two difference values, instabilityies from the effects of analog components in the ramp generator are canceled.

Please replace paragraph [0078] with the following replacement paragraph.

[0078] Figures 11A-11C illustrate a frequency locking process involving changing the slope of the ramp signal. Figure 11A illustrates an initial cycle involving a gentle slope. As illustrated, the period of the reference clock is considerably greater than the period of the feedback clock. The magnitude 700 of the rising ramp captured into register 631 is therefore considerably smaller than the magnitude 701 of the falling ramp captured into register

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632. Time duration 702 differs considerably from time duration 703.

Please replace paragraph [0083] with the following replacement paragraph.

[0083] The particulars of the frequency locked loop of Figure 9 are provided for illustrative purposes. Other frequency locked loop structures are known in the art and can be employed in microcontroller 600. Parts of the frequency locked loop circuitry of Figure 9 can be replaced with other circuitry as well. For example, Figure 12 illustrates circuitry that can be used in place of the coarse/fine demux/register block 637 and digitally controlled oscillator (DCO) block 638 of the embodiment of Figure 9. Namely, blocks 637 and 638 of the circuit of Figure 9 are replaced with a sigma delta modulator 712, digital-to-analog converter 713, low pass filter 714 and voltage controlled oscillator 715 as illustrated in Figure 12.